In the Specification:

Please amend the paragraph beginning at page 8, line 19 of the specification as follows:

A frame delay conversion circuit **106** is also provided to generate frame offsets. As illustrated by FIG. 3, the frame delay conversion circuit **106** may receive three (3) count bits (CNT<2:0>) and one phase bit from the frame alignment counter **102**. The combination of the phase bit and the three count bits may be treated as a frame delay byte, with the phase bit constituting the most significant bit therein. The frame delay conversion circuit **106** may perform a bit swap operation by inverting the value of the phase bit and moving the placement of the inverted phase bit from the most significant bit location to the least significant bit location. Thus, as illustrated by FIG. 2, an inverted value of the phase bit FD11 within a frame delay byte may be treated as the least significant bit DLEn of a four bit frame offset byte. If 4.5 clock cycles is the maximum acceptable frame offset at a rated speed of operation, for example, the range of acceptable frame offsets may extend from a value indicating no offset (i.e., {OFn2, OFn1 **[[**OFn2**]]**, OFn0, DLEn} = 0000) to a maximum acceptable offset of 4.5 clock cycles (i.e., {OFn2, OFn1 **[[**OFn2**]]**, OFn0, DLEn} = 1001). The frame delay conversion circuit **106** may also generate unacceptable frame offsets outside the ten acceptable values in the range from 0000 to 1001. These acceptable frame offsets (and possibly the unacceptable frame offsets in the remaining range from 1010 to 1111) are preferably written into an internal temporary register **110** using a temporary register write control circuit **108**. This temporary register write control circuit **108** is preferably responsive to a temporary register select signal that may be generated by a control counter **104**.